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PATENT

Attorney Docket No. B-3858DIV 620913-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant: Daniel Yap, et al

Patent Application No.: 10/649,075

Filed: 08/26/2003

For: "Optical Bond-Wire
Interconnections ..."

) On Appeal to the
) Board of Appeals

) Group Art Unit: 2872

) Examiner: Cherry, Euncha P

) Date: March 8, 2006
)

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Final rejection, dated August 10, 2005, for the above identified patent application. Appellants submit that this Appeal Brief is being timely filed, since the notice of Appeal was filed on January 10, 2006.

REAL PARTY IN INTEREST

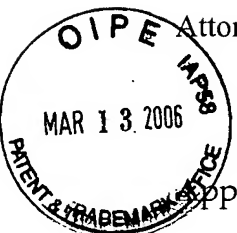
The present application has been assigned to HRL Laboratories, LLC of Malibu, CA.

RELATED APPEALS AND INTERFERENCES

Appellants submit that there are no other prior and pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-28 are currently pending, Claims 29-41 have been canceled without prejudice and Claims 42-43 are withdrawn without prejudice from consideration by the Examiner. Claims 1-28 are the subject of this Appeal and are reproduced in the accompanying Claims appendix.



STATUS OF AMENDMENTS

No Amendment After Final Rejection has been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

The invention described and claimed in the present application relates to the interconnection of microelectronic chips through the use of optical wires (p. 1, ll. 9-20).

According to the present application, optical wires (3) may be used to interconnect monolithic microwave integrated circuits (MMIC) (2) (p. 7, last paragraph to page 8, l. 7; Figure 1; Claim 1).

Claim 1 of the present disclosure is directed to an interconnection for interconnecting microelectronic chips (2) with optical wires (3), wherein said optical wires (3) are bonded onto said microelectronic chips (2) and optically connected therewith.

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Issue 1: Whether Claims 1-4, 6-8, 10, 13-14, 16, 23 and 25 are patentable under 35 U.S.C. 102(b) in view of Palmer, U.S. Patent No. 3,963,920, (hereinafter "Palmer")?

Issue 2: Whether Claims 5, 9, 11-12, 15, 17-22, 24 and 26-28 are patentable under 35 U.S.C. 103(a) in view of Palmer?

ARGUMENT

Issue 1: Whether Claims 1-4, 6-8, 10, 13-14, 16, 23 and 25 are patentable under 35 U.S.C. 102(b) in view of Palmer, U.S. Patent No. 3,963,920, (hereinafter "Palmer")?

In the final Office Action of August 10, 2005, the Examiner rejects Claims 1-4, 6-8, 10, 13-14, 16, 23 and 25 under 35 U.S.C. 102(b) as being anticipated by Palmer. Appellants respectfully disagree with the Examiner's rejection for the following reasons.

Claim 1

Appellants submit that the Examiner has not shown that Palmer discloses, suggests or teaches, *inter alia*, at least the following features recited by Claim 1 of the present application:

"optical wires are bonded onto said microchips and **optically connected** therewith " (emphasis added)

The Examiner asserts that the "optical wires" as recited in Claim 1 are disclosed by Palmer's "connector leads 33." See page 2, section 2 of the Official Action.

In response to Appellants' arguments that Palmer's connector leads "33" are metal and therefore cannot be considered as optical wires, the Examiner asserts that Palmer does not limit the leads to be only metal. See page 5, lines 2-8 of the final Office Action. According to the Examiner, because Palmer discloses "glass/metal feedthrough," Palmer discloses leads that can be glass. Appellants respectfully traverse the Examiner's erroneous assertions.

Appellants respectfully bring to the Appeal Board's attention U.S. Patent No. 6,788,873 issued to Fritz. According to Fritz, the "term 'glass/metal feedthrough' is generally understood in electronics and electrical engineering to be a vacuum-tight seal or fusion of glass to metal for passing an **electrical conductor or conductors** in an insulating fashion through a hermetically encapsulated housing" (emphasis added). See column 4, lines 24-31 of Fritz enclosed in the Evidence appendix.

Therefore, based on the generally understood definition of the term "glass/metal feedthrough" as stated in, *inter alia*, the U.S. Patent cited above, the glass/metal feedthrough disclosed in Palmer **cannot possibly be** the "optical wires" recited in Claim 1, as mistakenly asserted by the Examiner.

It is more likely that Palmer uses glass/metal feedthroughs to pass electrical connector leads "33" through the hermetically sealed enclosure "10." See Figure 1

of Palmer. This is further supported by the fact that Palmer discloses using wire bond leads that connect leads "33" to the substrate "30." See Figure 2 of Palmer. Applicants note that the wire bond leads connecting leads "33" to the substrate "30" are identical to wire bond leads "22" shown in Figure 2 of Palmer.

Therefore, Palmer does not teach, disclose or suggest that "optical wires are bonded onto said microchips and optically connected therewith" as recited in Claim 1, because Palmer's leads "33" are **not** "optical wires" as recited in Claim 1. Hence, Claim 1 is patentable over Palmer and the Examiner's rejection should be reversed on appeal.

Claims 2-4, 6-8, 10, 13-14, 16, 23 and 25

Claims 2-4, 6-8, 10, 13-14, 16, 23 and 25, at least based on their dependency on Claim 1, are also patentable over Palmer.

Issue 2: Whether Claims 5, 9, 11-12, 15, 17-22, 24 and 26-28 are patentable under 35 U.S.C. 103(a) in view of Palmer?

In the final Office Action of August 10, 2005, the Examiner rejects Claims 5, 9, 11-12, 15, 17-22, 24 and 26-28 under 35 U.S.C. 103(a) as being obvious in view of Palmer. Appellants respectfully disagree with the Examiner's rejection for the following reasons.

Appellants submit that, at least for the reasons stated above for Claim 1, the Examiner has **not** established a *prima facie* case of obviousness for the claims rejected under 35 U.S.C. §103(a). Claims 5, 9, 11-12, 15, 17-22, 24 and 26-28, at least based on their dependency on Claim 1, are also patentable over Palmer. Appellants respectfully request that the Examiner's rejection be reversed on appeal.

* * *

Conclusion

For the extensive reasons advanced above, Appellant respectfully contends that each claim is patentable. Therefore, reversal of all rejections and objections is courteously solicited.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this Appeal Brief is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

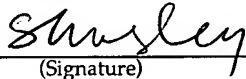
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March 8, 2006

(Date of Mailing)

Shannon Tinsley

(Name of Person Mailing)



(Signature)

March 8, 2006

(Date)

Respectfully submitted,



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1. (Original) An interconnection for interconnecting microelectronic chips with optical wires, wherein said optical wires are bonded onto said microelectronic chips and optically connected therewith.
 2. (Previously presented) The interconnection according to Claim 1, wherein at least one optical wire of said optical wires comprises a segment of an optical fiber, said segment having two opposite ends, said ends being a first end and a second end, said ends being attached to said microelectronic chips by means of terminations, said terminations being disposed on a substrate material having a first side and a second side.
 3. (Original) The interconnection according to Claim 2, said terminations being optically coupled to said optical fiber and said terminations being further electrically coupled to said microelectronic chips.
 4. (Original) The interconnection according to Claim 2, wherein said terminations comprise a laser chiplet and a photodetector chiplet, said first end being connected to said laser chiplet and said second end being connected to said photodetector chiplet.
 5. (Original) The interconnection according to Claim 2, wherein said optical fiber is having a numerical aperture of at least about 0.35.
 6. (Original) The interconnection according to Claim 2, further comprising a groove and a mirror.
 7. (Original) The interconnection according to Claim 2, wherein said optical fiber is disposed within a groove.
 8. (Original) The interconnection according to Claim 3, wherein said terminations are vertically coupled devices.
 9. (Original) The interconnection according to Claim 3, wherein said terminations further comprise solder bumps and gold/gold compression bonds.

10. (Original) The interconnection according to Claim 4, wherein an optical path is established so that light travels from said laser chiplet through said substrate material to said photodetector chiplet.

11. (Original) The interconnection according to Claim 4, wherein said terminations are having a size of not more than about 250 micrometers in width and not more than about 250 micrometers in length.

12. (Original) The interconnection according to Claim 4, wherein said laser chiplet comprises a vertical-cavity surface emitting laser.

13. (Original) The interconnection according to Claim 4, wherein said photodetector chiplet comprises a PIN photodiode detector or a metal-silicon-metal photodetector.

14. (Original) The interconnection according to Claim 6, wherein said mirror is disposed on said second side of said terminations.

15. (Original) The interconnection according to Claim 6, wherein said second side of said substrate is a (100) crystallographic surface, said groove is aligned along (011) crystallographic direction and said mirror is aligned along (011) crystallographic direction.

16. (Original) The interconnection according to Claim 7, wherein said groove is V-shaped.

17. (Original) The interconnection according to Claim 9, wherein said electrical coupling of said terminations to said microelectronic chips is achieved with two or more of said solder bumps or said compression bonds.

18. (Original) The interconnection according to Claim 10, wherein said substrate material comprises gallium arsenide or indium phosphide.

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19. (Original) The interconnection according to Claim 10, wherein said substrate material has a Zinc-blende crystallographic structure.
20. (Original) The interconnection according to Claim 12, wherein said vertical-cavity surface emitting laser is fabricated on a gallium arsenide substrate.
21. (Original) The interconnection according to Claim 12, wherein said vertical-cavity surface emitting laser is fabricated on an indium phosphide substrate.
22. (Original) The interconnection according to Claim 12, wherein said vertical-cavity surface emitting laser is disposed on said first side of said terminations.
23. (Original) The interconnection according to Claim 13, wherein said photodetector chiplets are disposed on said first side of said terminations.
24. (Original) The interconnection according to Claim 13, wherein said photodetector chiplets are fabricated on a substrate material, said substrate material comprising gallium arsenide or indium phosphide.
25. (Original) The interconnection according to Claim 16, wherein said groove is disposed on said second side of said termination.
26. (Original) The interconnection according to Claim 20, wherein said vertical-cavity surface emitting laser emits at a wavelength selected from a group of wavelengths, said group comprising wavelengths of about 980 nanometers or about 1300 nanometers.
27. (Original) The interconnection according to Claim 21, wherein said vertical-cavity surface emitting laser emits at a wavelength selected from a group of wavelengths, said group comprising wavelengths of about 1300 nanometers or about 1550 nanometers.

28. (Original) The interconnection according to Claim 24, wherein said photodetector chiplets are sensitive within a range of wavelengths between about 980 nanometers and about 1550 nanometers.

29-41 (Canceled)

42. (Withdrawn) An optical interconnection for connecting an optical fiber to an integrated circuits by an optical fiber, the integrated circuit including an integrated circuit substrate and a chiplet mounted on the integrated circuit substrate for connection to said optical fiber, the chiplet having:

- (a) a chiplet substrate with a termination device arranged on one side of the chiplet;
- (b) the optical fiber being disposed on another side of the chiplet substrate, the another side of the chiplet including an inclined surface for reflecting light through the chiplet and from the termination device to the optical fiber or from the optical fiber to the termination device.

43. (Withdrawn) The interconnection according to claim 1 wherein said microelectronic chips include an integrated circuit substrate and a chiplet mounted on the integrated circuit substrate for connection to said optical wires, the chiplet having:

- (a) a chiplet substrate with a termination device arranged on one side of the chiplet;
- (b) the optical wire being disposed on another side of the chiplet substrate, the another side of the chiplet including an inclined surface for reflecting light through the chiplet and from the termination device to the optical wire or from the optical wire to the termination device.

A definition of the term "glass/metal feedthrough" from U.S. Patent No. 6,788,873 is enclosed herein. The definition of the term "glass/metal feedthrough" from U.S. Patent No. 6,788,873 was entered in the record with the response, dated November 7, 2005, to the final Office Action dated August 10, 2005.